

**NT140WHM-N51****HW:V8.0****Final Product Specification****Rev. 0****BOE Optoelectronics Technology Co., Ltd**

**REVISION HISTORY**

( ) Preliminary Specification

(√) Final Specification

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## 1.0 GENERAL DESCRIPTION

### 1.1 Introduction

NT140WHM-N51 V8.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 14.0 inch diagonally measured active area with HD resolutions (1366 horizontal by 768 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262k(6bit) colors and color gamut 45%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

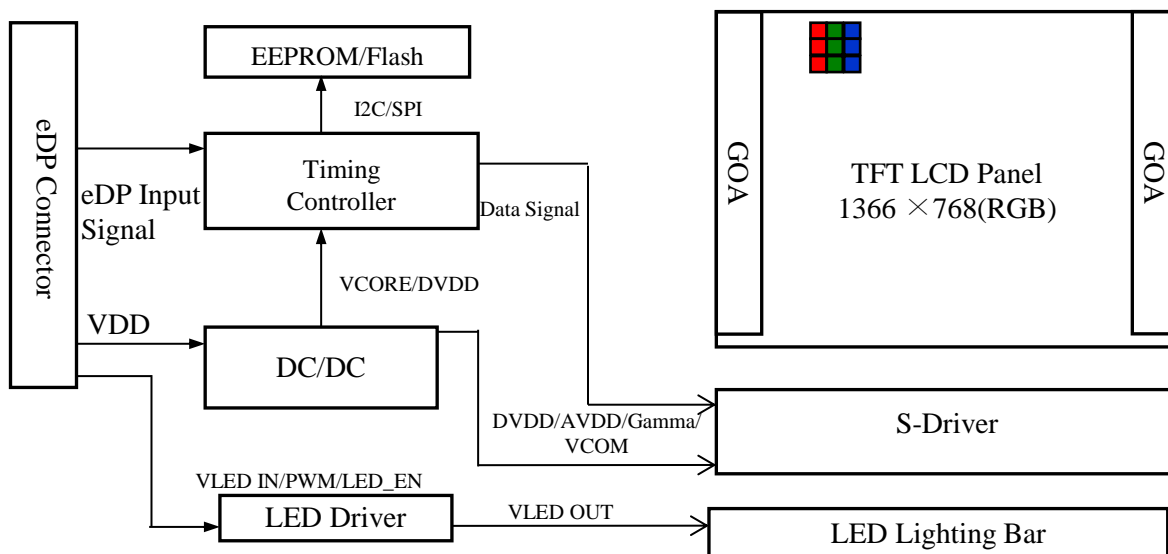


Figure 1. Drive Architecture

### 1.2 Features

- 1 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 262k(6bit) color depth, color gamut 45%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.1

### 1.3 Application

- Notebook PC (Wide type)

### 1.4 General Specification

The followings are general specifications at the model NT140WHM-N51 V8.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	309.4(H) × 173.95(V)	mm	
Number of pixels	1366 (H) × 768 (V)	pixels	
Pixel pitch	75.46(H) *226.29(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	262k(6bit)		
Color gamut	45%		
Display mode	Normally White		
Dimensional outline	315.9 ± 0.3 (H)*186.05 ± 0.3(V)(W/O PCB)*3.0 (Max) 315.9 ± 0.3(H)*197.55 ± 0.5(V) (W/PCB)*3.0(Max)	mm	
Weight	285(max)	g	
Surface treatment	HC		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P <sub>D</sub> : 0.7(Max)	W	@Mosaic
	P <sub>BL</sub> : 2.7(Max)	W	
	P <sub>Total</sub> : 3.4(Max)	W	@Mosaic

Notes : 1. LED Lighting Bar (32\*LED Array)

## 2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings >

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V <sub>DD</sub>	-0.3	4.0	V	Note 1
eDP input Voltage	V <sub>eDP</sub>	0	2.0	V	
Logic Supply Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V	
Operating Temperature	T <sub>OP</sub>	0	+50	°C	Note 2
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	

Notes :

1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.

2. Temperature and relative humidity range are shown in the figure below.

95 % RH Max. ( 40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C ) No condensation.

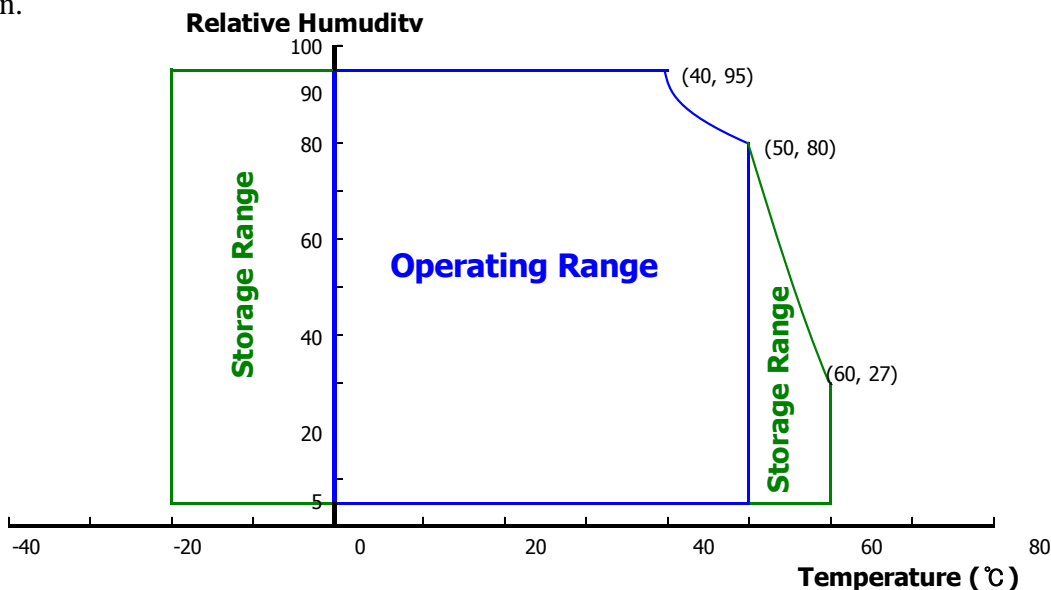


Figure 2. Temperature and Relative Humidity Range

### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.1 Electrical Specifications

< Table 3. Electrical Specifications >

Ta=25+/-2°C

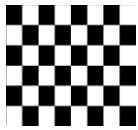
Parameter		Min.	Typ.	Max.	Unit	Remarks	
Power Supply Voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	Note 1	
Permissible Input Ripple Voltage	V <sub>RF</sub>	-10% VDD	-	+10% VDD	V	@ V <sub>DD</sub> = 3.3V	
Power Supply Inrush Current	Inrush	-	-	1.5	A	Note3	
Power Supply Current	Mosaic	I <sub>DD</sub>	-	142	212	mA	Note 1
	RGB		-	232	273	mA	
Power Consumption	Mosaic	P <sub>M</sub>	-	0.469	0.7	W	
	RGB	P <sub>RGB</sub>	-	0.766	0.9	W	
	BLU	P <sub>BL</sub>	-	2.076	2.7	W	Note 2
	Total	P <sub>Total</sub>	-	2.842	3.6	W	@Mosaic

## 3.0 ELECTRICAL SPECIFICATIONS

### 3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.  
The current draw and power consumption specified is for 3.3V at 25 °C.
  - a) Mosaic pattern 8\*8
  - b) R/G/B patterns



(a)



(b)

Figure 3. Power Measure Patterns

2. Calculated value for reference ( $V_{LED} \times I_{LED}$ )
3. Measure condition (Figure 4)

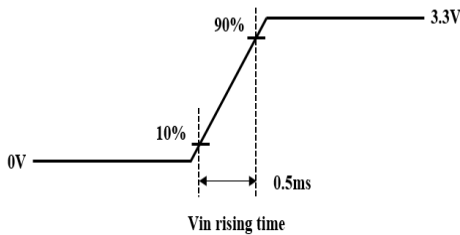


Figure 4. Inrush Measure Condition



### 3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications >

Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks	
LED Forward Voltage	V <sub>F</sub>	-	-	2.9	V		
LED Forward Current	I <sub>F</sub>	-	20	-	mA		
LED Power Input Voltage	V <sub>LED</sub>	5	12	21	V		
LED Power Input Current	I <sub>LED</sub>	-	-	225	mA	Note 1	
LED Power Consumption	P <sub>LED</sub>	-	-	2.7	W		
Power Supply Voltage for LED Driver Inrush	I <sub>led</sub> inrush	-	-	1.5	A	Note 3	
LED Life-Time	N/A	15,000	-	-	Hour	I <sub>F</sub> = 20mA Note 2	
EN Control Level	Backlight On	V <sub>BL_EN</sub>	2.2	-	3.6	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	High Level	V <sub>BL_PWM</sub>	2.2	-	3.6	V	
	Low Level		0	-	0.5	V	
PWM Control Frequency	F <sub>PWM</sub>	200	-	2,000	Hz		
Duty Ratio		5	-	100	%		

Notes :

1. Power supply voltage 12V for LED driver.  
Calculator value for reference  $I_F \times V_F \times 32 / \text{driver efficiency} = P_{LED}$
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

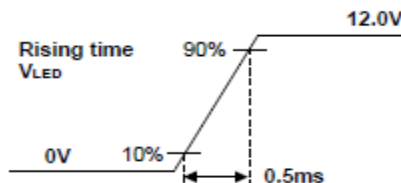


Figure 5. Inrush Measure Condition

### 3.3 LED Structure

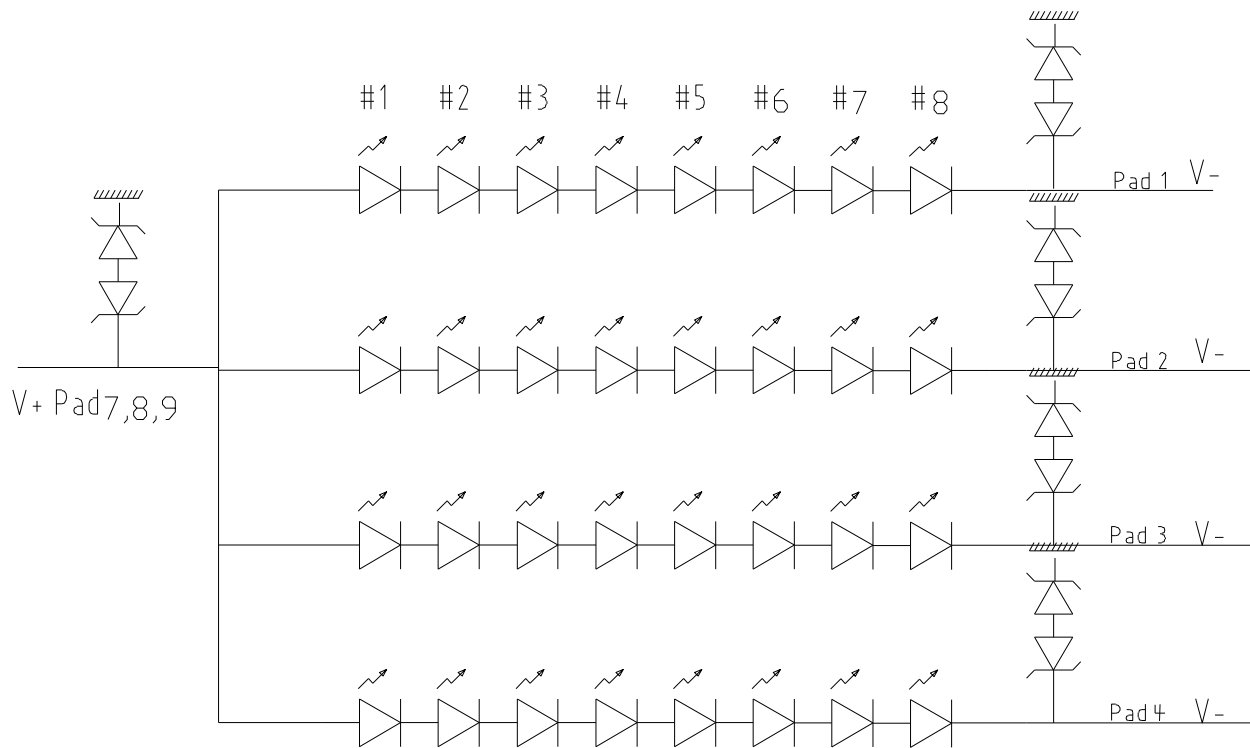


Figure 6. LED Structure

## 4.0 OPTICAL SPECIFICATION

### 4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance  $\leq 1$  lux and temperature =  $25 \pm 2^\circ\text{C}$ ) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of  $\theta$  and  $\Phi$  equal to  $0^\circ$ . We refer to  $\theta=0$  ( $=\theta_3$ ) as the 3 o'clock direction (the "right"),  $\theta=90$  ( $=\theta_{12}$ ) as the 12 o'clock direction ("upward"),  $\theta=180$  ( $=\theta_9$ ) as the 9 o'clock direction ("left") and  $\theta=270$  ( $=\theta_6$ ) as the 6 o'clock direction ("bottom"). While scanning  $\theta$  and/or  $\Phi$ , the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be  $3.3 \pm 0.3\text{V}$  at  $25^\circ\text{C}$ . Optimum viewing angle direction is 6 o'clock.

### 4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	$\theta_3$	CR > 10	-	45	-	Deg.	Note 1
		$\theta_9$		-	45	-	Deg.	
	Vertical	$\theta_{12}$		-	20	-	Deg.	
		$\theta_6$		-	40	-	Deg.	
Luminance Contrast Ratio		CR	$\theta = 0^\circ$	300	500	-		Note 2
Luminance of White	5 Points	$Y_w$	$\theta = 0^\circ$ ILED = 20mA	212.5	250	-	cd/m <sup>2</sup>	Note 3
White Luminance Uniformity	5 Points	$\Delta Y_5$		80	-	-	%	Note 4
	13 Points	$\Delta Y_{13}$		62.5	-	-	%	
White Chromaticity		$W_x$	$\theta = 0^\circ$	0.283	0.313	0.343		Note 5
		$W_y$		0.299	0.329	0.359		
Reproduction of Color	Red	$R_x$	$\theta = 0^\circ$	Typ.-0.03	0.589	Typ.+0.03		
		$R_y$			0.343			
	Green	$G_x$			0.330			
		$G_y$			0.570			
	Blue	$B_x$			0.157			
		$B_y$			0.137			
Color Gamut				-	45	-	%	
Response Time (Rising + Falling)		$T_{RT}$	$T_a = 25^\circ\text{C}$ $\theta = 0^\circ$	-	12	16	ms	Note 6
Cross Talk		CT	$\theta = 0^\circ$	-	-	2.0	%	Note 7

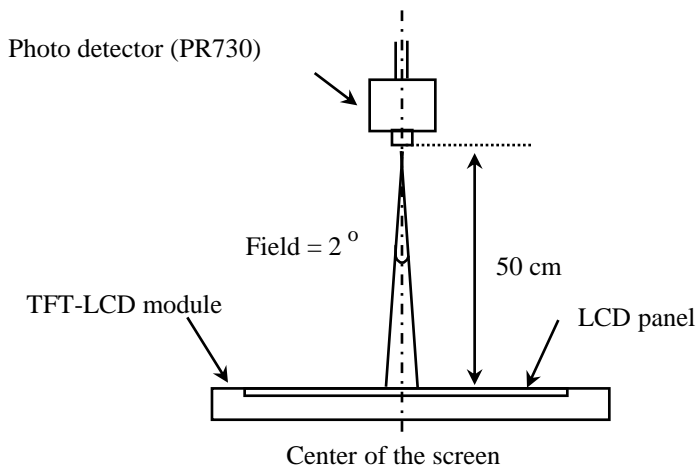
## Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).
2. Contrast measurements shall be made at viewing angle of  $\Theta = 0$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as :  $\Delta Y = \text{Minimum Luminance of 5(or 13) points} / \text{Maximum Luminance of 5(or 13) points.}$ (see Figure 8 and Figure 9).
5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. The electro-optical response time measurements shall be made as Figure 10 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_r$ .
7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a  $10 \pm 1$ mm diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark. The luminance ratio shall not exceed 1:1.05 (See Figure 11).

### 4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

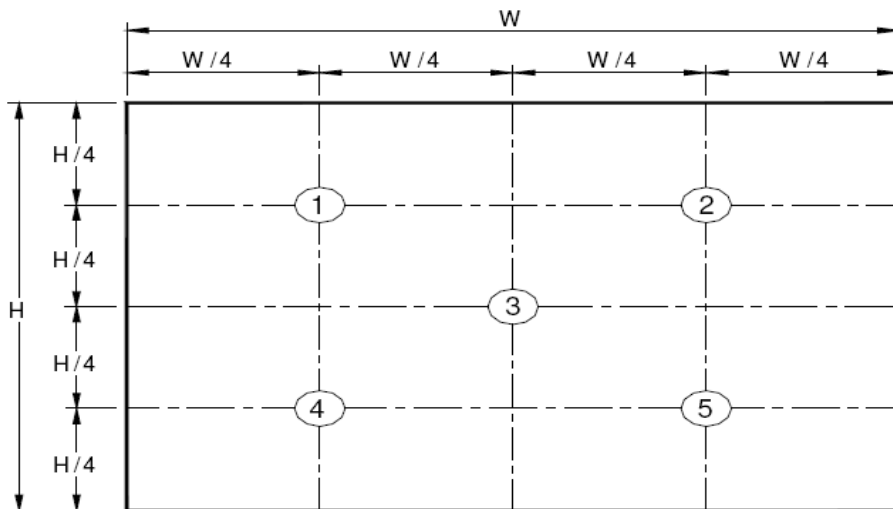


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

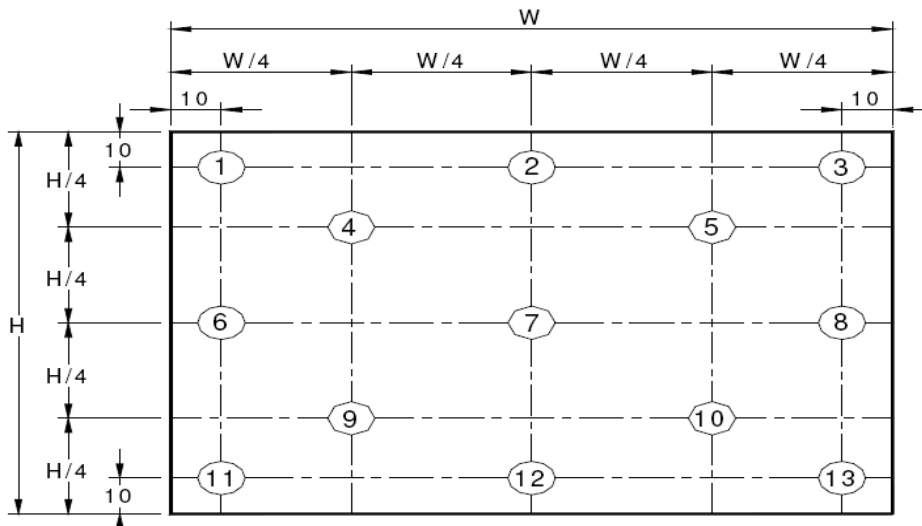


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as :  $\Delta Y5$  = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) ,  $\Delta Y13$  = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

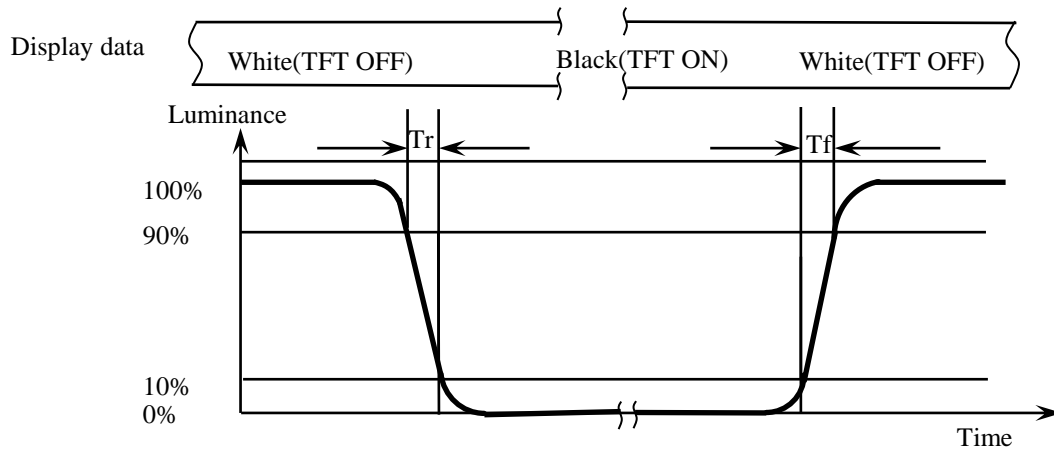
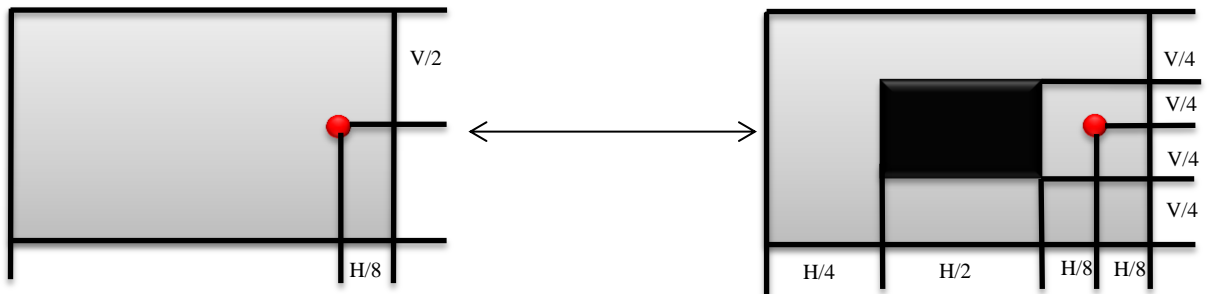


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the “data” input signal ON and OFF.  $T_r$ : The luminance to change from 90% to 10% , $T_f$ : The luminance to change from 10% to 90% .

The test system : LMS PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

$Y_A$  = Initial luminance of measured area (cd/m<sup>2</sup>)

$Y_B$  = Subsequent luminance of measured area (cd/m<sup>2</sup>)

The location measured will be exactly the same in both patterns. The test background gray is L127.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance ( $Y_A$ ) of a  $10 \pm 1$ mm diameter area, with all display pixels set to a gray level 127, to the luminance ( $Y_B$ ) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

## 5.0 INTERFACE CONNECTION

### 5.1 Electrical Interface Connection

The electronics interface connector is STM MSAK24025P30.

The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	No Connection
2	H_GND	Ground
3	NC	No Connection
4	NC	No Connection
5	H_GND	Ground
6	LANE0_N	eDP RX channel 0 negative
7	LANE0_P	eDP RX channel 0 positive
8	H_GND	Ground
9	AUX_CH_P	eDP AUX CH positive
10	AUX_CH_N	eDP AUX CH negative
11	H_GND	Ground
12	LCD_VCC	Power Supply, 3.3V (typ.)
13	LCD_VCC	Power Supply, 3.3V (typ.)
14	NC	No Connection
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot plug detect output
18	BL_GND	LED Ground
19	BL_GND	LED Ground
20	BL_GND	LED Ground
21	BL_GND	LED Ground
22	BL_ENABLE	LED enable pin(+3.3V Input)
23	BL_PWM	System PWM Signal Input
24	NC	No Connection
25	NC	No Connection
26	BL_POWER	LED Power Supply 5V-21V
27	BL_POWER	LED Power Supply 5V-21V
28	BL_POWER	LED Power Supply 5V-21V
29	BL_POWER	LED Power Supply 5V-21V
30	NC	No Connection



## 5.2 eDP Interface

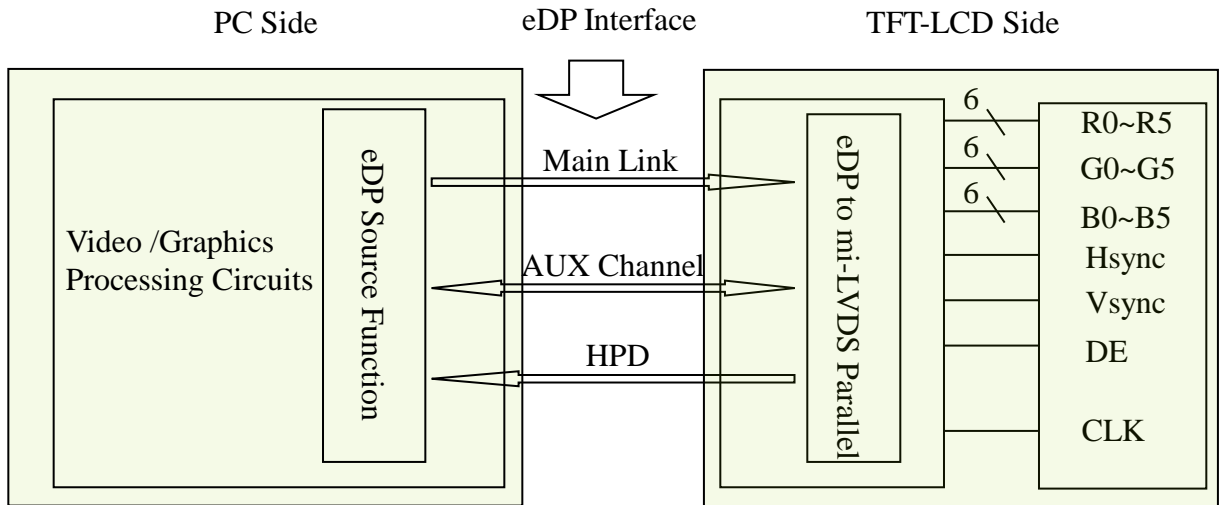


Figure 12. eDP Interface Architecture

**Note:**

Transmitter : Parade DP501 or equivalent.

Transmitter is not contained in module.

### 5.3 Data Input Format

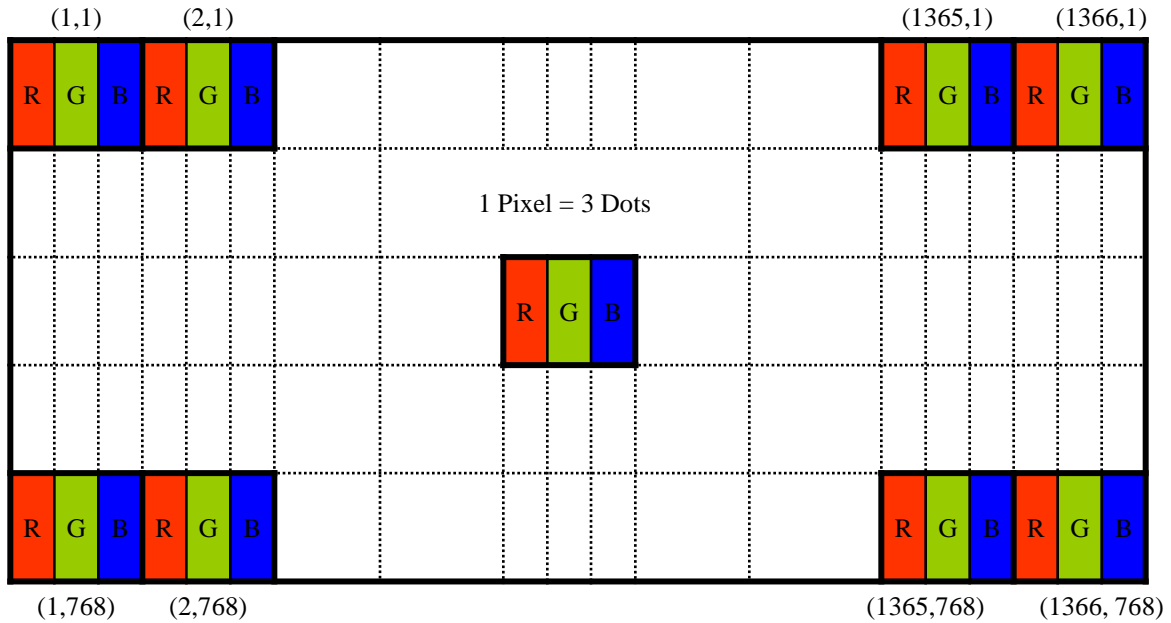


Figure 13. Display Position of Input Data (V-H)

**5.4 Back-light & LCM Interface Connection**

BLU Interface Connector: STM MSK24022P10 .

&lt;Table 7. Pin Assignments for the BLU Connector&gt;

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	LED	LED cathode connection	6	NC	No Connection
2	LED	LED cathode connection	7	NC	No Connection
3	LED	LED cathode connection	8	Vout	LED anode connection
4	LED	LED cathode connection	9	Vout	LED anode connection
5	NC	No Connection	10	Vout	LED anode connection

## 6.0 SIGNAL TIMING SPECIFICATION

### 6.1 The NT140WHM-N51 V8.0 Is Operated By The DE Only

< Table 8. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	77.54	78.41	79.30	MHz
Frame Period		Tv	818	823	828	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	768	-	lines
One line Scanning Period		Th	1580	1588	1596	clocks
Horizontal Display Period		Thd	-	1366	-	clocks

Note : The above is as optimized setting.

## 6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 9. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	100	-	1320	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	-	120	$\Omega$	
Single-ended termination resistance	RRX-SE	40	-	60	$\Omega$	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_INTRA_PAIR	-	-	60	ps	
AC Coupling Capacitor	CSOURCE_ML	75		200	nF	Source side

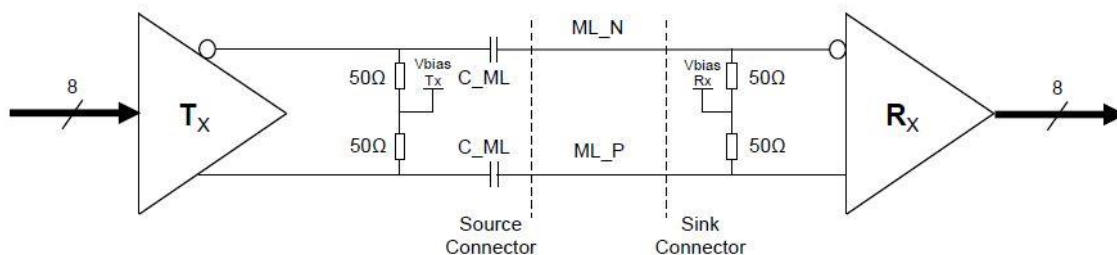


Figure 14. Main link differential pair

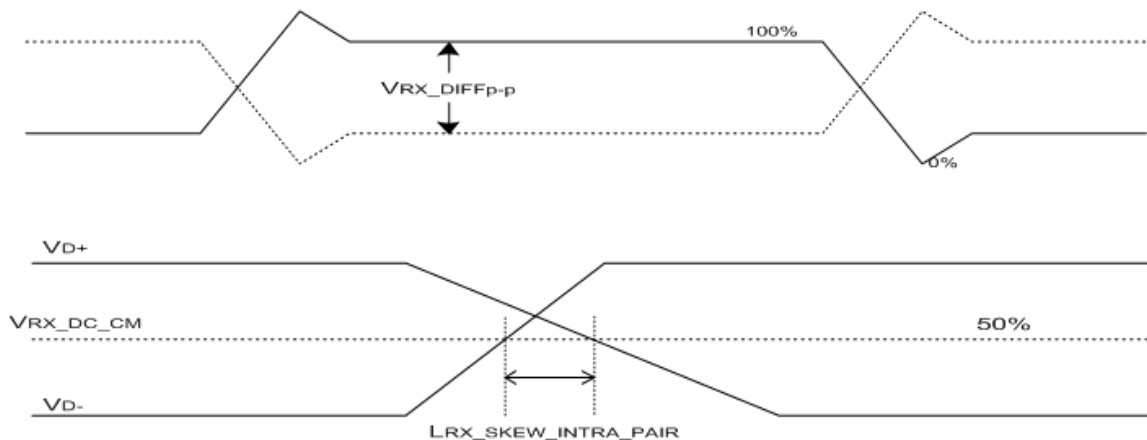


Figure 15. VRX-DIFFp-p & LRX\_SKEW\_INTRA\_PAIR

<Table 10. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V <sub>HPD</sub>	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

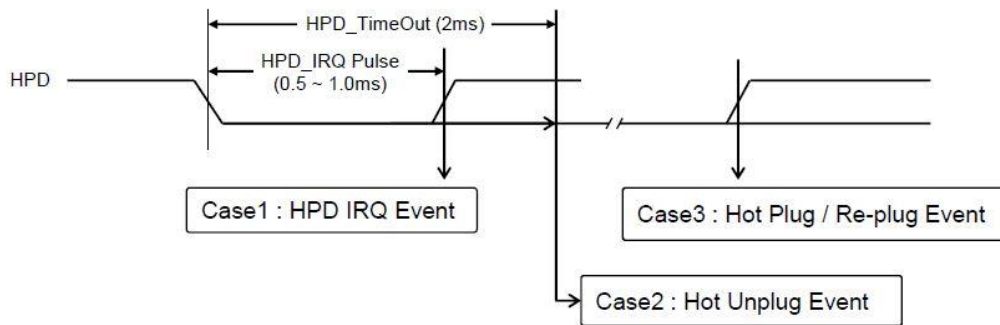


Figure 16. HPD Events

<Table 11. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

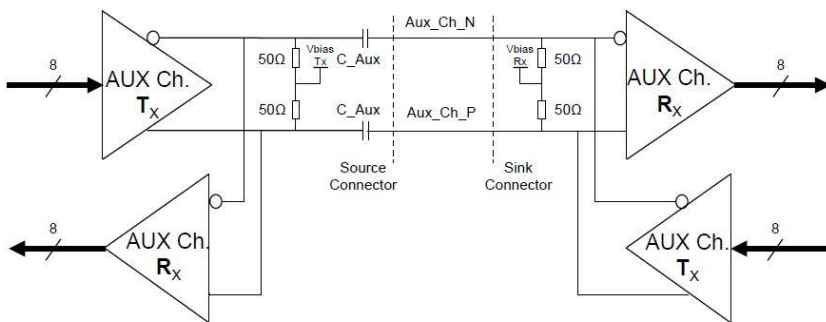


Figure 17. AUX differential pair



## 7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△				↑						?						↑		
	▽				↓						?						↓		
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△				↑						↑						↑		
	▽				↓						↓						↓		
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	White	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

## 8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

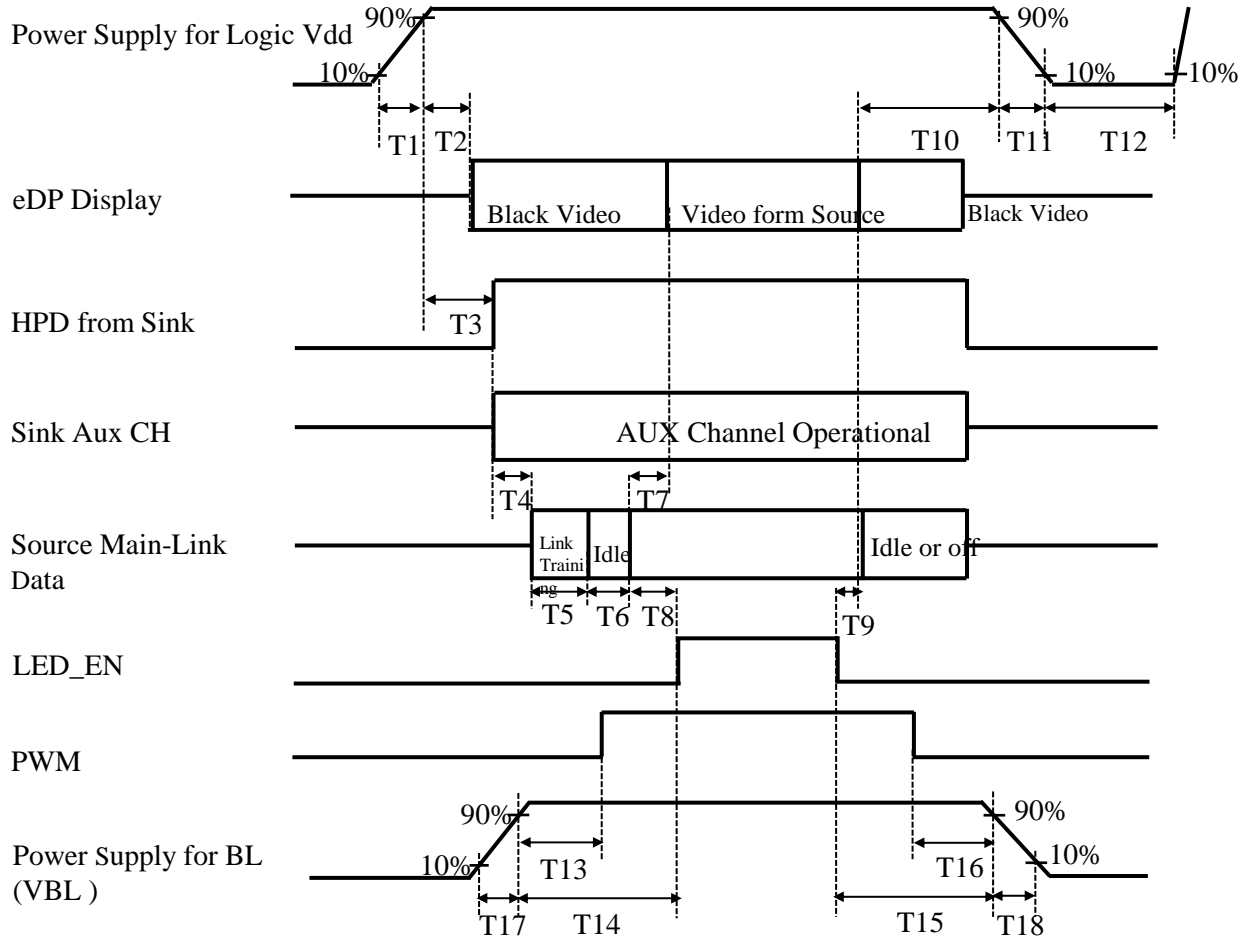


Figure 18. Power Sequence

- $0.5\text{ms} \leq T1 \leq 10 \text{ ms}$
- $0\text{ms} < T2 \leq 200 \text{ ms}$
- $0\text{ms} < T3 \leq 200 \text{ ms}$
- $T4+T5+T6+T8 > 80\text{ms}$
- $0\text{ms} < T7 \leq 50\text{ms}$
- $50\text{ms} < T8$
- $0\text{ms} < T9$
- $0\text{ms} < T10 < 500 \text{ ms}$
- $0.5\text{ms} \leq T11 \leq 10 \text{ ms}$
- $500\text{ms} \leq T12$
- $0\text{ms} < T13$
- $0\text{ms} < T14$
- $0\text{ms} < T15$
- $0\text{ms} < T16$
- $0.5\text{ms} \leq T17$
- $0.5\text{ms} \leq T18$

Notes:

- When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
- Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

## 9.0 Connector Description

Physical interface is described as for the connector on LCM.

These connectors are capable of accommodating the following signals and will be following components.

### 9.1 TFT LCD Module

< Table 13. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	STM
Type/ Part Number	MSAK24025P30
Mating Housing/ Part Number	20455-030E-66

## 10.0 MECHANICAL CHARACTERISTICS

### 10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NT140WHM-N51 V8.0.  
Other parameters are shown in Table 14.

<Table 14. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	309.4(H) × 173.95(V)	mm
Number of pixels	1366 (H) × 768 (V)	pixels
Pixel pitch	75.46(H) * 226.29(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally white	
Dimensional outline	315.9 ± 0.3 (H) * 186.05 ± 0.3 (V) (W/O PCB) * 3.0 (Max) 315.9 ± 0.3 (H) * 197.55 ± 0.5 (V) (W/PCB) * 3.0 (Max)	mm
Weight	285(max)	g

### 10.2 Mounting

See Figure 23.

### 10.3 Glare and Polarizer Hardness.

The surface of the LCD has a Glare coating to minimize reflection and to reduce scratching.

The Polarizer Hardness is 3H.

### 10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

**11.0 RELIABILITY TEST**

The reliability test items and its conditions are shown in below.

<Table 15. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 60% ± 3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ± 15 KV Contact : 150 pF, 330Ω, ± 8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

## 12.0 HANDLING & CAUTIONS

### (1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

### (2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

### (3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

### (4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

### (5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

### (6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

## 13.0 LABEL

### (1) Product Label



Figure 19. Product Label

### Module ID Naming Rule:

<Table 16. Module ID Naming Rule>

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year	Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ						

(2) High voltage caution label

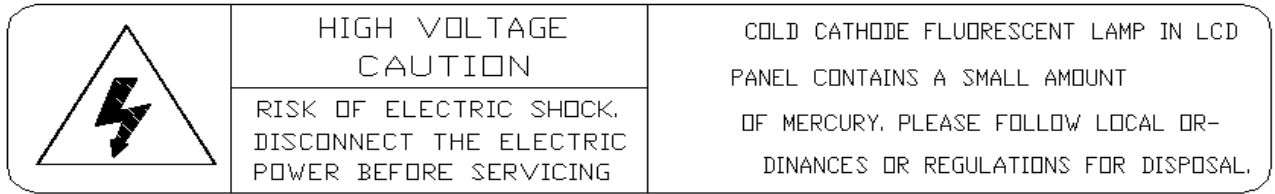


Figure 20. High Voltage Caution Label

(3) Box label

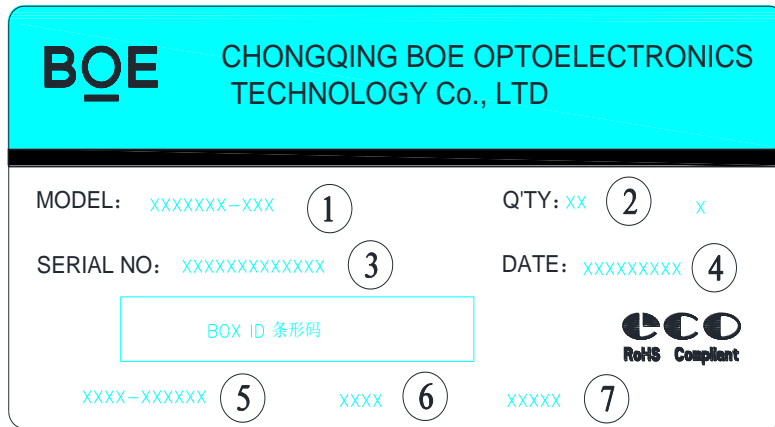


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

Total Size:100×50mm

<Table 17. Box Label Naming Rule >

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				



## 14.0 PACKING INFORMATION

### 14.1 Packing Order

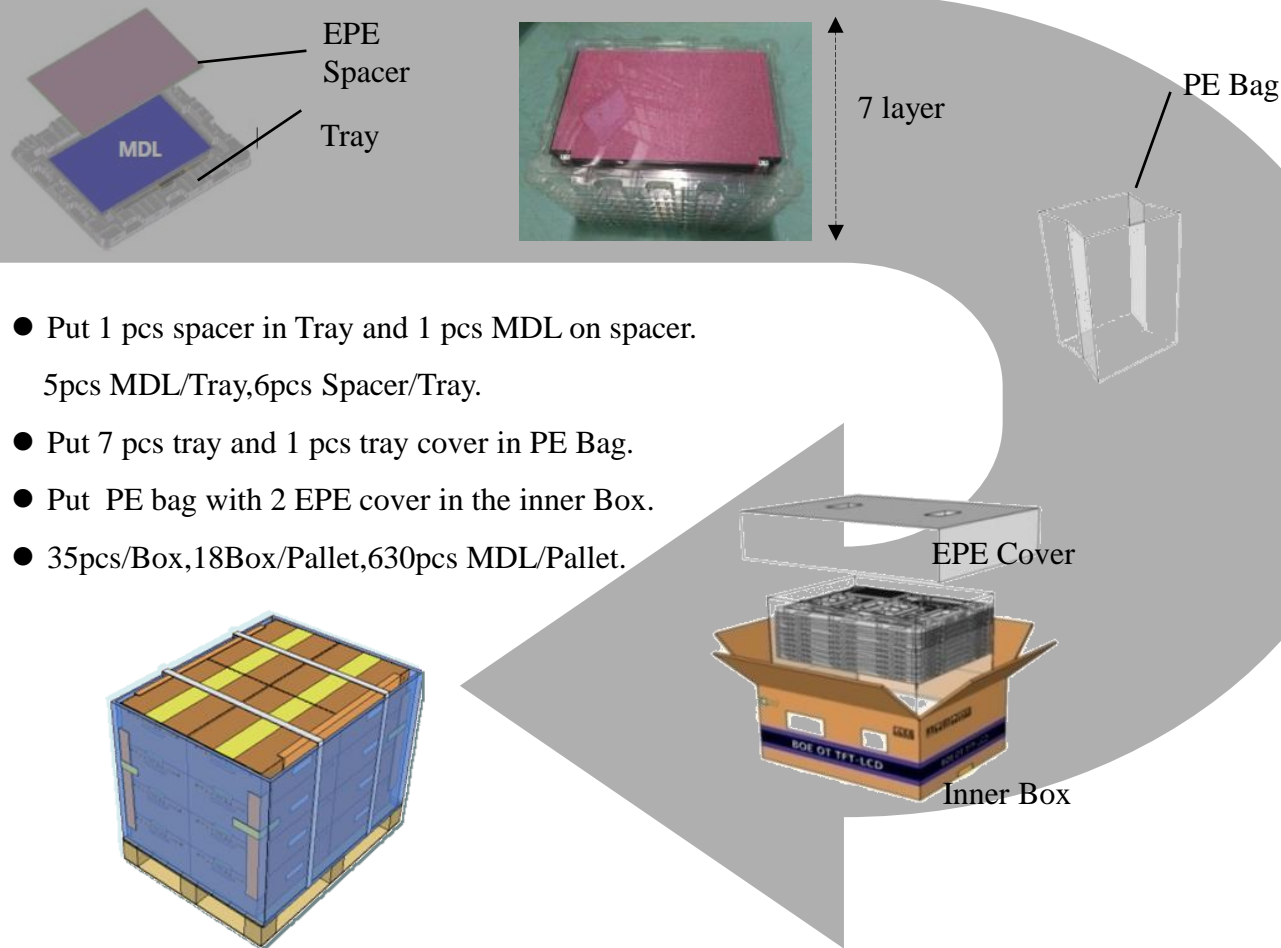


Figure 22. Packing Order

### 14.2 Note

- Box dimension: 480mm\*350mm\*285mm
- Package quantity in one box: 35pcs
- Total weight: 12.6 kg/Box (Typ.)

## 15.0 MECHANICAL OUTLINE DIMENSION

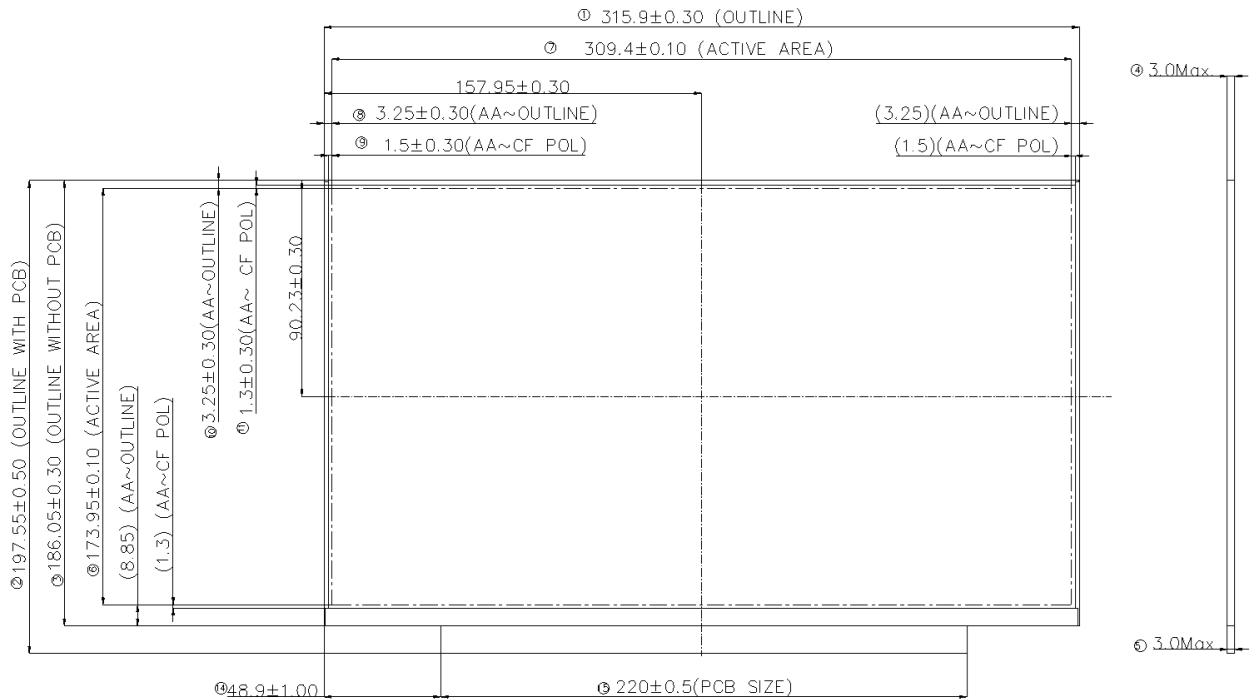


Figure 23. TFT-LCD Module Outline Dimension (Front View)

### Notes:

1. Warpage and deformation Spec.: 0.5mm Max..
2. The eDP connector is measured at PIN 1 and mating line.
3. Unspecified tolerance refer to  $\pm 0.3$  mm.
4. Top polarizer is the highest portion.
5. Critical dimension: ① ~ ⑩ CPK: ① ~ ⑤
6. Do not have light leakage on four corners of module.
7. Measurement method refer to Appendix A
8. System matching refer to Appendix B
9. “( )”marks the reference dimensions.

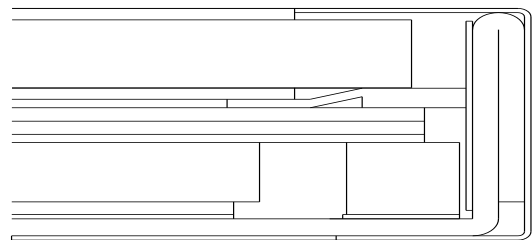


Figure 24. Highest Point Position

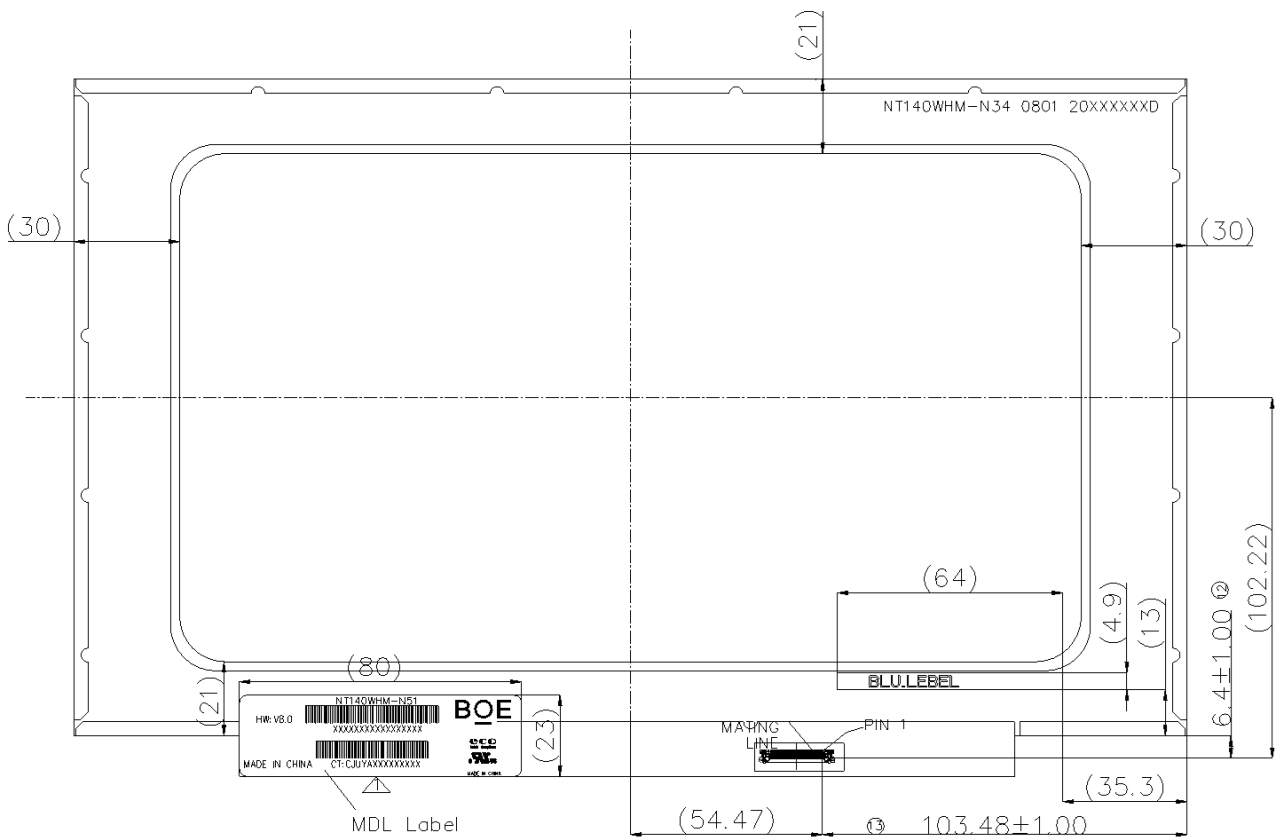


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

Notes:

1. Warpage and deformation Spec.: 0.5mm Max..
2. The eDP connector is measured at PIN 1 and mating line.
3. Unspecified tolerance refer to  $\pm 0.3$  mm.
4. Top polarizer is the highest portion.
5. Critical dimension: ① ~ ⑩ CPK: ① ~ ⑤
6. Do not have light leakage on four corners of module.
7. Measurement method refer to Appendix A
8. System matching refer to Appendix B
9. “( )”marks the reference dimensions.

## 16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	2B	43		2347	ID = 2347
0B		09	9			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	0B	11		11	
11	Year of Manufacture	1E	30		2020	Manufactured in 2020
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	95	149		-	Refer to right table
15	Max H image size	1F	31		31	30.94 cm (Approx)
16	Max V image size	11	17		17	17.395 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	03	3		-	Refer to right table
19	Red/Green low bits	F8	248		-	Red / Green Low Bits
1A	Blue/White low bits	45	69		-	Blue / White Low Bits
1B	Red x high bits	96	150	603	0.589	Red (x) = 10010110 (0.589)
1C	Red y high bits	57	87	351	0.343	Red (y) = 01010111 (0.343)
1D	Green x high bits	54	84	338	0.330	Green (x) = 01010100 (0.33)
1E	Green y high bits	92	146	584	0.570	Green (y) = 10010010 (0.57)
1F	Blue x high bits	28	40	161	0.157	Blue (x) = 00101000 (0.157)
20	Blue y high bits	23	35	140	0.137	Blue (y) = 00100011 (0.137)
21	White x high bits	50	80	321	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	337	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	A2	162		78.4	78.41544MHz Main clock
37		1E	30			
38		56	86		1366	Hor Active = 1366
39		DE	222		222	Hor Blanking = 222
3A		50	80		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		00	0		768	Ver Active = 768
3C		37	55		55	Ver Blanking = 55
3D		30	48		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		36	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		35	53		309	Horizontal Image Size = 309.4 mm (Low 8 bits)
43		AE	174		174	Vertical Image Size = 173.95 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47	1A	26		-	Refer to right table	

48	Detailed timing/monitor descriptor #2	6C	108		52.3	52.27696MHz Main clock
49		14	20			
4A		56	86		1366	Hor Active = 1366
4B		DE	222		222	Hor Blanking = 222
4C		50	80		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		00	0		768	Ver Active = 768
4E		37	55		55	Ver Blanking = 55
4F		30	48		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48		48	Hor Sync Offset = 48
51		20	32		32	H Sync Pulse Width = 32
52		36	54		3	V sync Offset = 3 line
53		00	0		6	V Sync Pulse width : 6 line
54		35	53		309	Horizontal Image Size = 309.4 mm (Low 8 bits)
55		AE	174		174	Vertical Image Size = 173.95 mm (Low 8 bits)
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26		-	Refer to right above table
5A		Detailed timing/monitor descriptor #3	00	0		Nvidia nvDPS (Refer the tab of nvDPS)  Lowest refresh rate that does not cause any visual/optical side effect
5B	00		0			
5C	00		0			
5D	00		0			
5E	00		0			
5F	00		0			
60	00		0			
61	00		0			
62	00		0			
63	00		0			
64	00		0			
65	00		0			
66	00		0			
67	00	0				
68	00	0				
69	00	0				
6A	00	0				
6B	00	0				

6C	Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4
6D		00	0			Flag
6E		00	0			Reserved
6F		02	2			For Brightness Table and Power consumption
70		00	0			Flag
71		0D	13		-	PWM % [7:0] @ Step 0
72		40	64		-	PWM % [7:0] @ Step 5
73		FF	255		-	PWM % [7:0] @ step 10
74		0A	10		-	Nits [7:0] @ Step 0
75		3C	60		-	Nits [7:0] @ Step 5
76		7D	125		-	Nits [7:0] @ Step 10
77		11	17		-	Panel Electronics Power @32x32 Chess Pattern = 700mW
78		11	17		-	Backlight Power @60 nits = 686.117647058824mW
79		21	33		-	Backlight Power @Step 10 = 2700mW
7A		7D	125		-	Nits @ 100% PWM Duty = 250nit
7B		00	0			Format :
7C	00	0			terminate with ASCII code 0Ah	
7D	00	0			and pad field with ASCII code 20h	
7E	Extension flag	00	0		1	
7F	Checksum	<b>5A</b>	<b>90</b>	<b>90</b>	-	

## 17.0 GENERAL PRECAUTIONS

### 17.1 HANDLING

(1) When the module is assembled, It should be attached to the system firmly using every mounting holes.

Be careful not to twist or bend the modules.

(2) Refrain from strong mechanical shock or any force to the module. Otherwise, it may cause improper operation or damage to the module.

(3) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than 1 HB pencil lead.

(4) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static , it may cause damage to the module.

(9) Use fingerstalls with soft gloves to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Do not pull or fold the LED FPC.

(12) Do not touch any component which is located on the back side.

(13) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(14) Pins of connector shall not be touched directly with bare hands.

### 17.2 STORAGE

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.



**17.3 OPERATION**

- (1) Do not connect, disconnect the module in the “ Power On” condition.
- (2) Power supply should always be turned on/off by following item 8.0 “ Power on/off sequence “.
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (4) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, BOE is not to be held reliable for the defective operations. It is strongly recommended to contact BOE to find out fitness for a particular purpose.

**17.4 OTHERS**

- (1) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (2) Do not exceed the absolute maximum rating value. ( the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.
- (3) If the module displays the same pattern continuously for a long period of time, it can be the situation when The “ image sticks” to the screen.
- (4) This module has its circuitry PCB’s on the rear or bottom side and should be handled carefully to avoid being stressed.

## Appendix A

## The Measurement Methods for the Dimensions of Module

## Caliper:

- a. Length of Outline
- b. Width of Outline (Without/With PCB)
- c. Thickness of Outline (Without/ With PCB)

## Coordinate Measuring Machine:

CF Polarizer Size

Active Area Size

Active Area to Outline (Without Tape Wrinkle or Bulged)

Active Area to CF Polarizer

The Distance of Bracket Holes

P-Cover to Outline (Without Tape Wrinkle or Bulged)

Length of P-Cover

Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

Height Gauge: The Different Height of Root and Top on the Bracket  
(Need to Calculate From Bracket Angle Spec.)

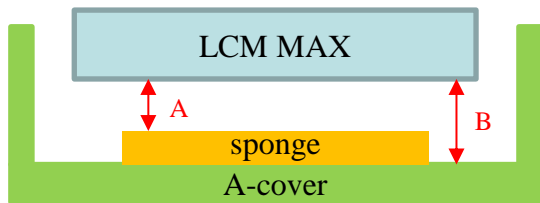
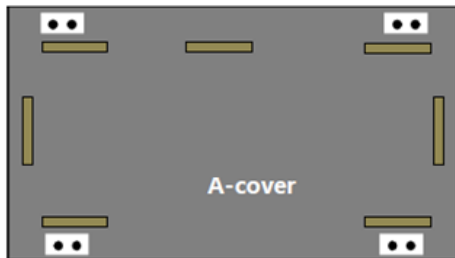
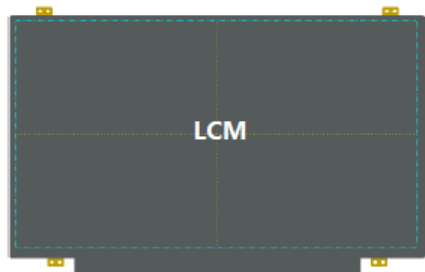
Feeler Gauge: The Warpage Spec. of Module

## Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.

Appendix B

## LCM to A-Cover / sponges z-gap



	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

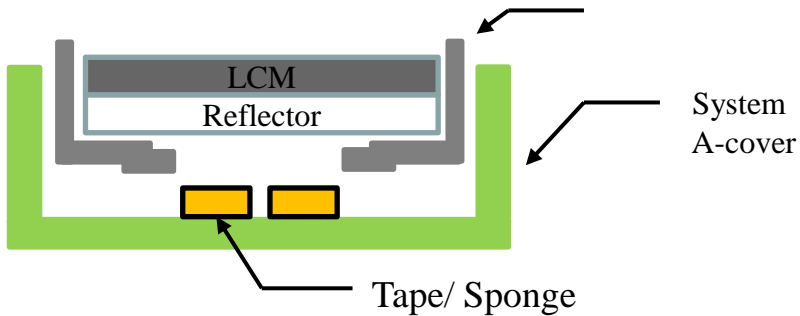
Purpose

The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water ripple, white spot and other abnormal display

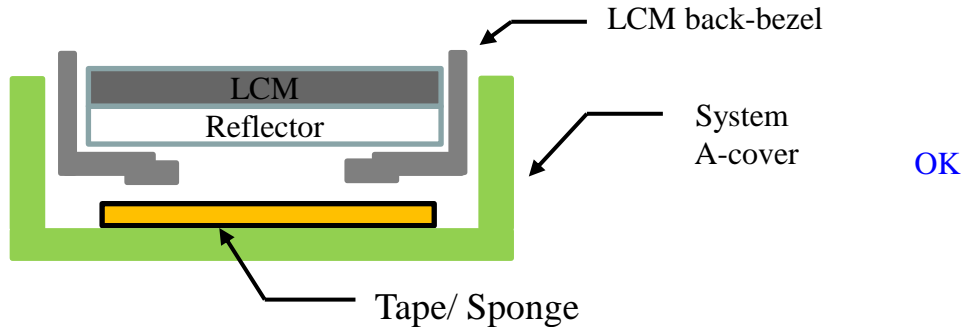
Appendix B

**LCM to A-Cover / sponges z-gap**

a



b

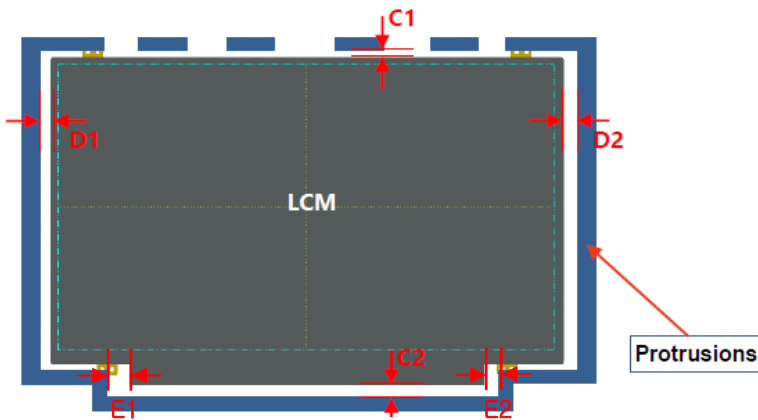


Purpose

If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

**LCM to side wall / protrusions**



	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose

We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display...etc. in the reliability test

Appendix B

## LCM to B-cover z-gap



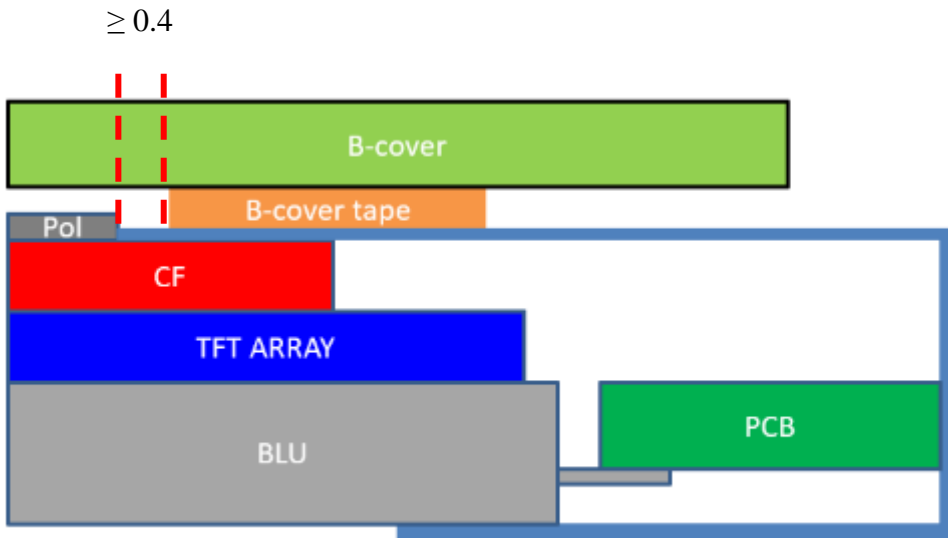
B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose

Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

Appendix B

**B-cover tape to top pol edge**



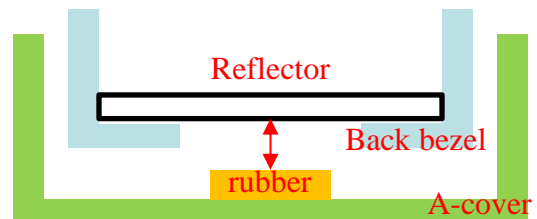
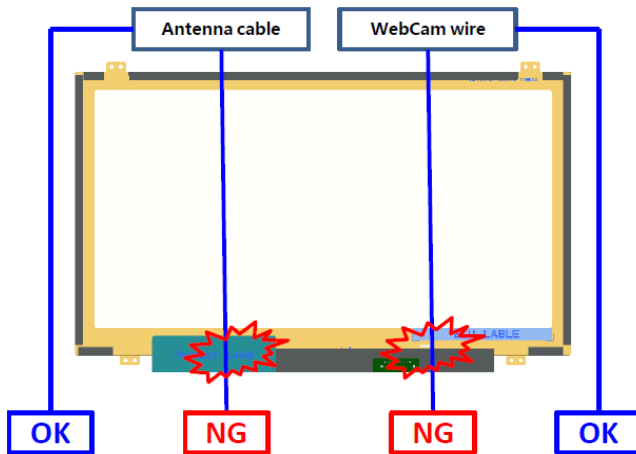
If attach b-cover and LCM with tapes,  
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose

To avoid the B-cover tape override top pol and cause pooling or light leakage issue

Appendix B

## Antenna Cable & Webcam wire



If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

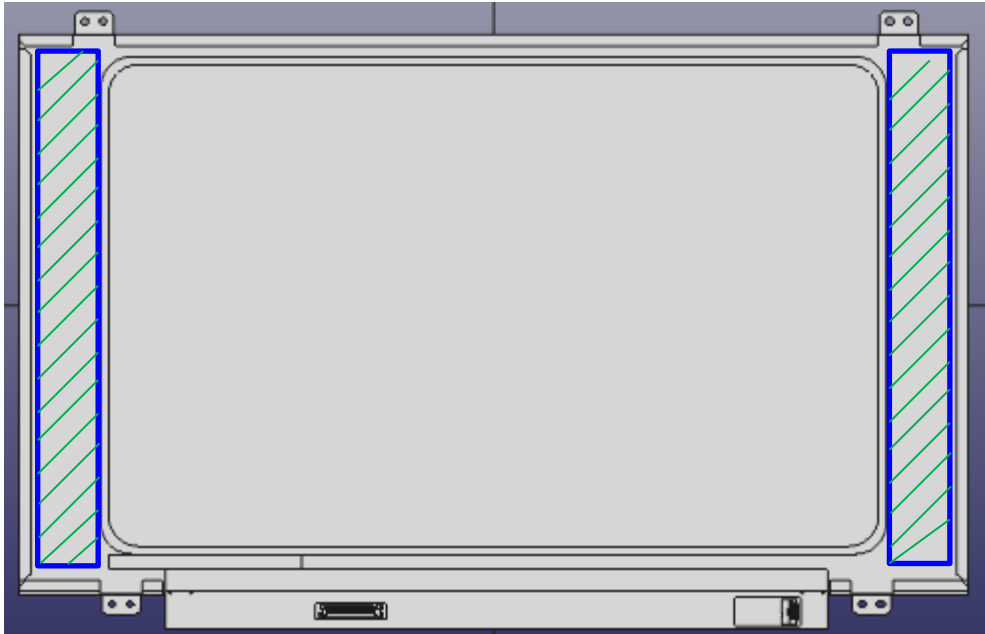
Purpose

1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display
2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubbers adjacent to the cable / wire route
3. Suggest that attach the cable / wire with tapes to A-cover
4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues



## Appendix B

### LCM paste area



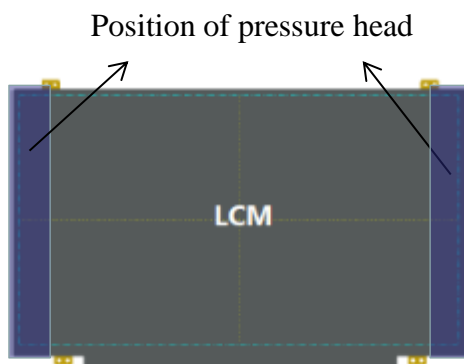
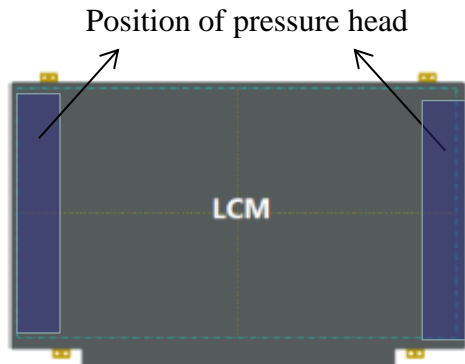
Attachment area

#### Purpose

If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

**LCM pressable area**

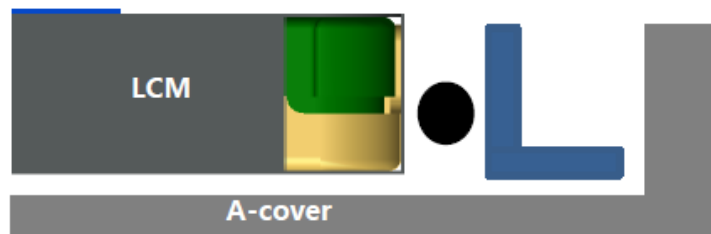
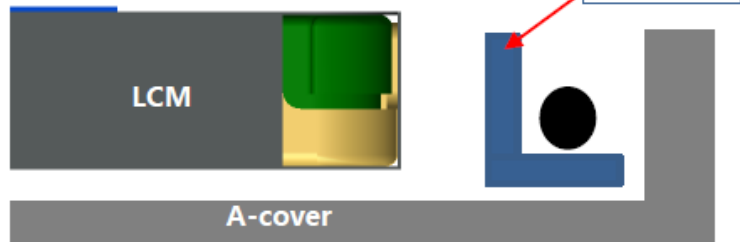
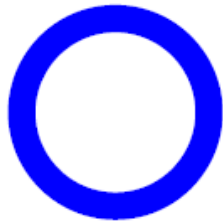


Purpose

1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling.
2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

## Wire setting

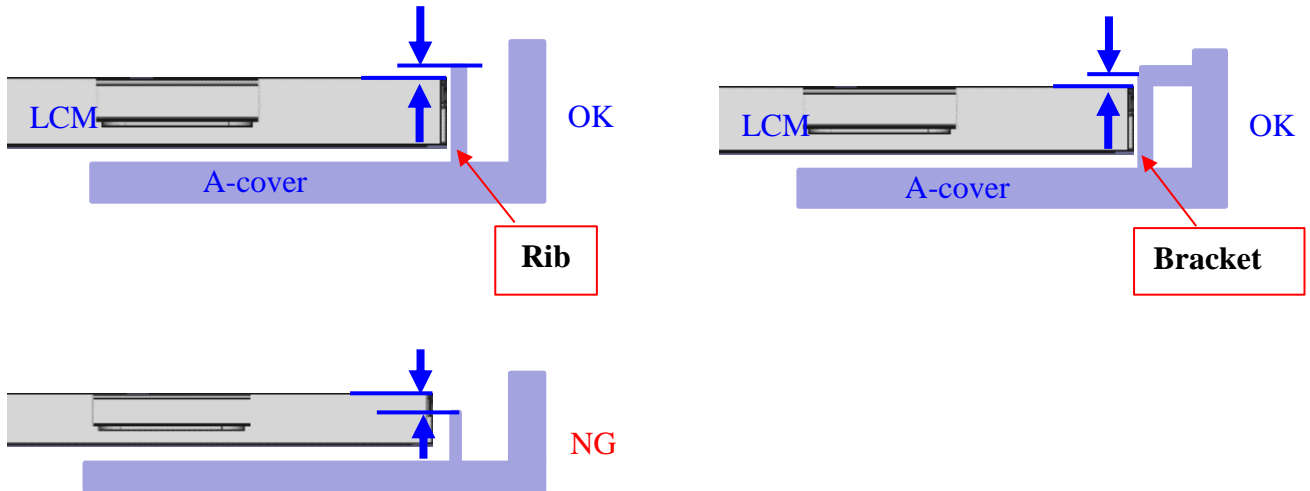


Purpose

Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.

Appendix B

## A-cover strength

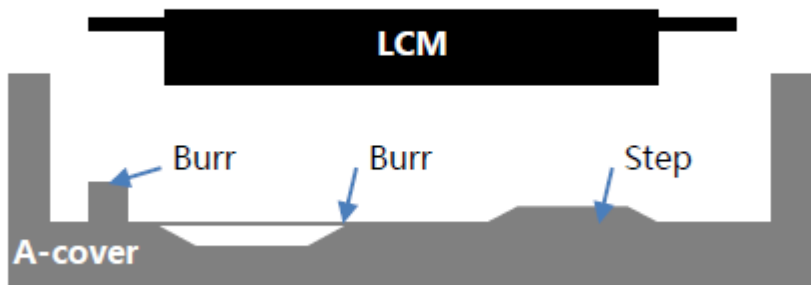


Purpose

1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels.
2. As for LCM is more stronger than Rib, the L Bracket is be recommended.

Appendix B

**System A-cover Inner Surface**

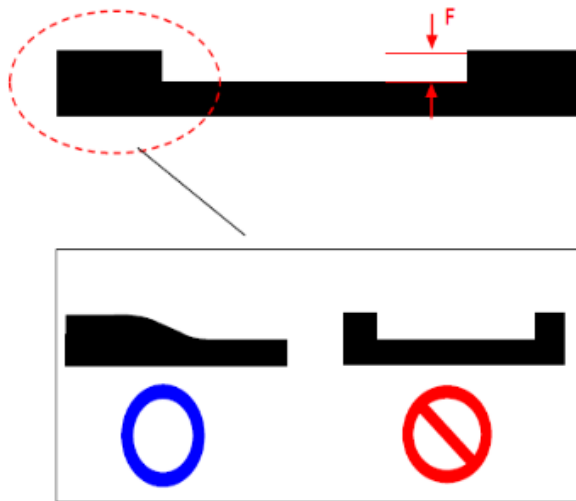
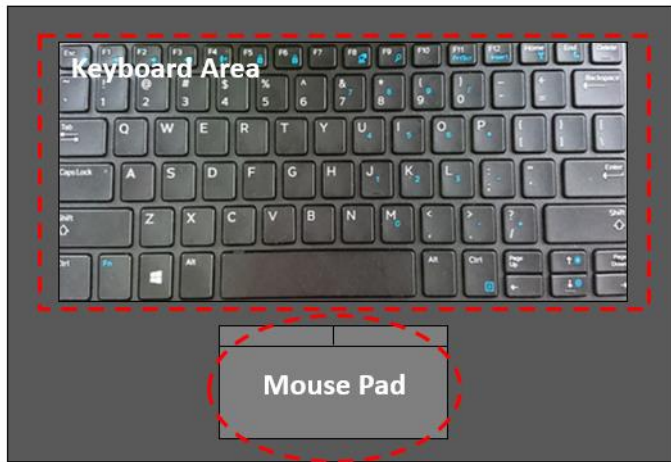


Purpose

There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.

Appendix B

## Keyboard area & Mouse pad



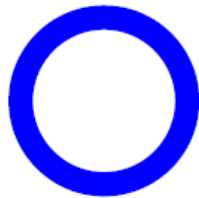
➤ F: max 0.3mm

Purpose

In order to avoiding LCM fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Pogo testing, if the broken hole is done in this location, it is easy to produce fragments.

Appendix B

## System cover reliability

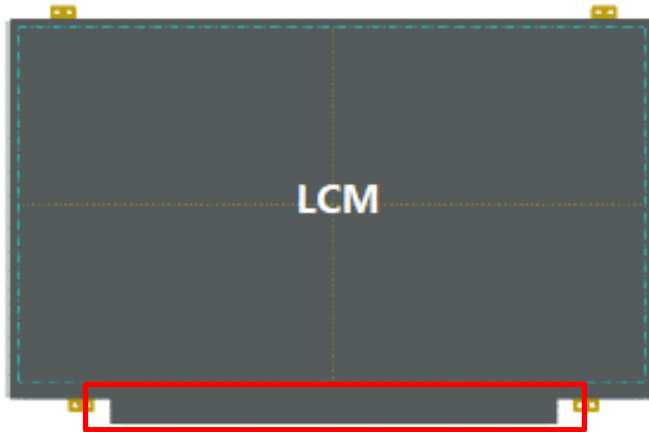


Purpose

The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.

## Appendix B

### A/B-cover near LCD PCBA



No magnetic object

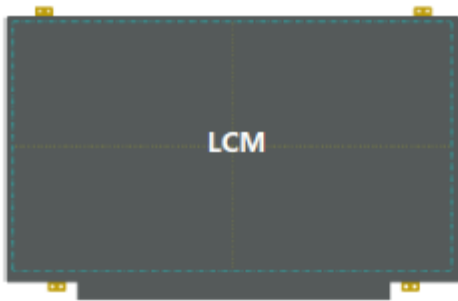
#### Purpose

There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue



Appendix B

**A-cover add sponges on Boss side wall**

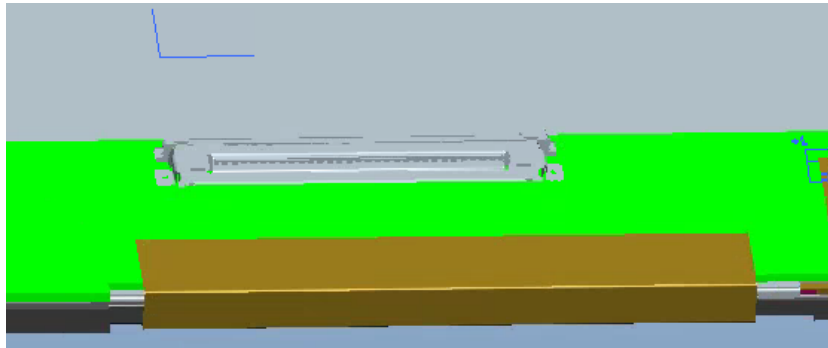
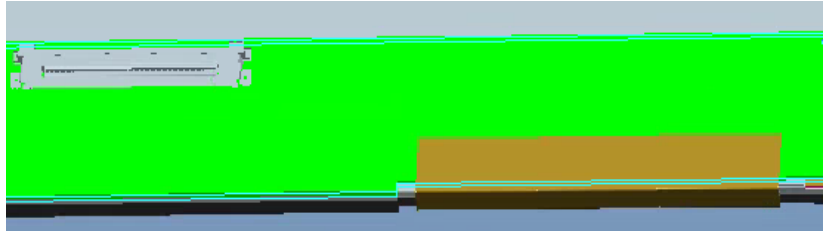
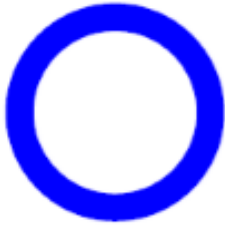


**Purpose**

We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

Appendix B

### LCM to A-Cover / sponges z-gap

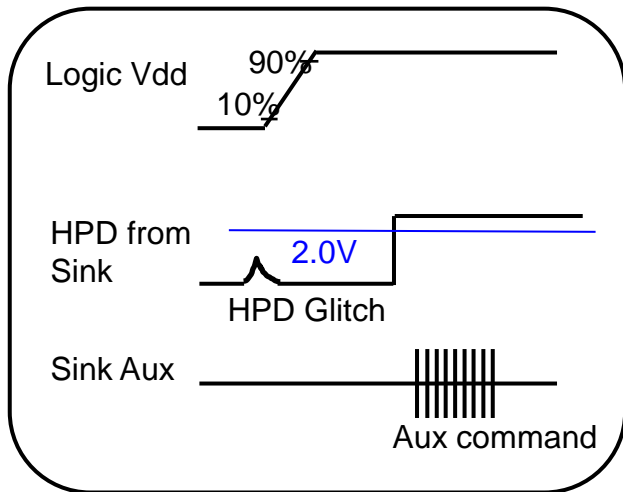


**Purpose**

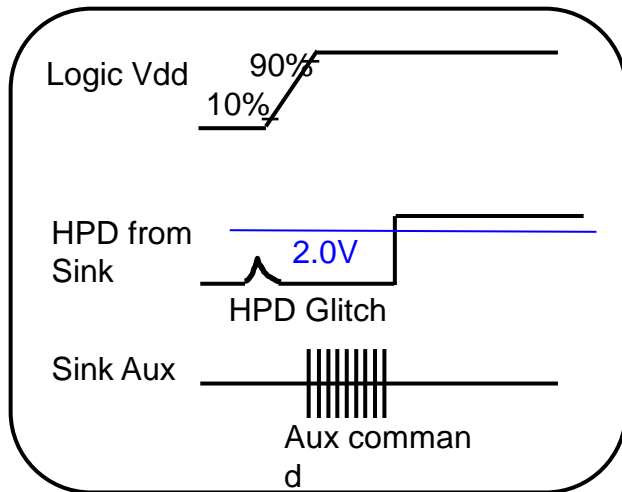
Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

## HPD Signal recognition



Normal Signal (Ignore HPD Glitch)



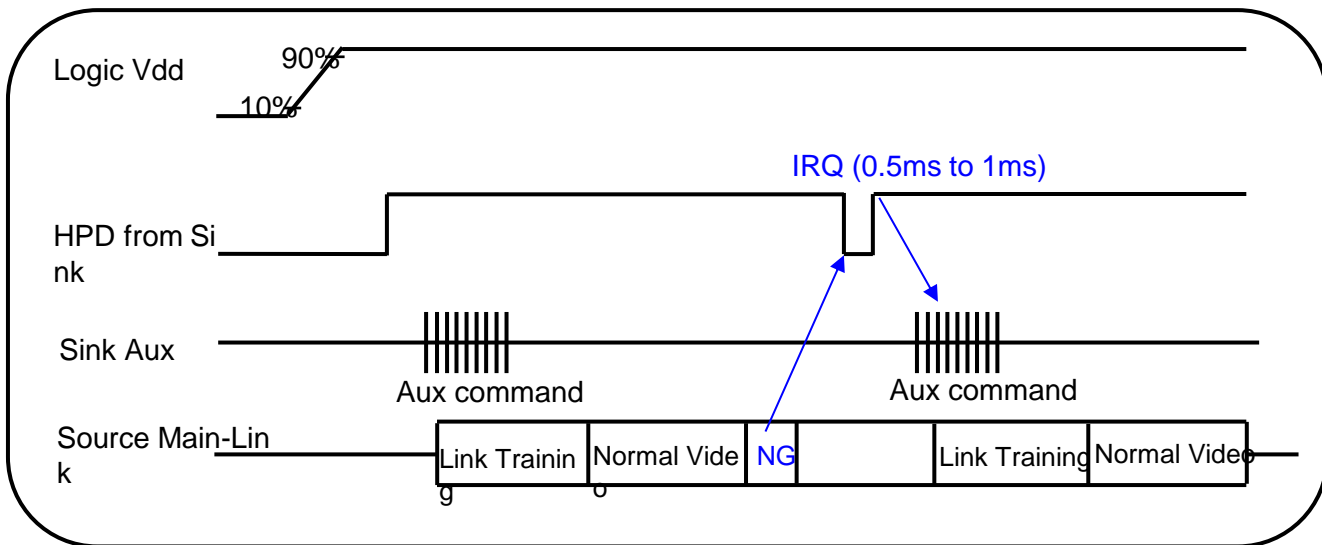
Abnormal Signal

Purpose

When HPD glitch of source device minimum is 2.0(V).

Appendix C

## HPD Signal Definition IRQ (Interrupt Request)

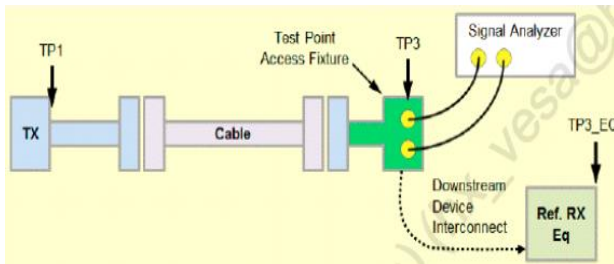


**Purpose**

When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

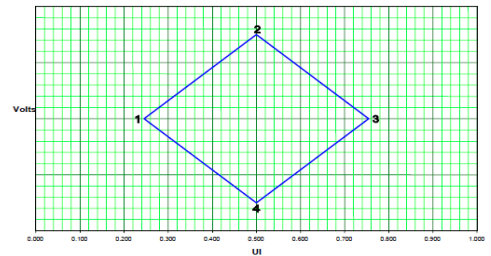
## Main link eye diagram of TP3



Measured TP3 on LCM connector.

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR



Downstream Device Mask at TP3

	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

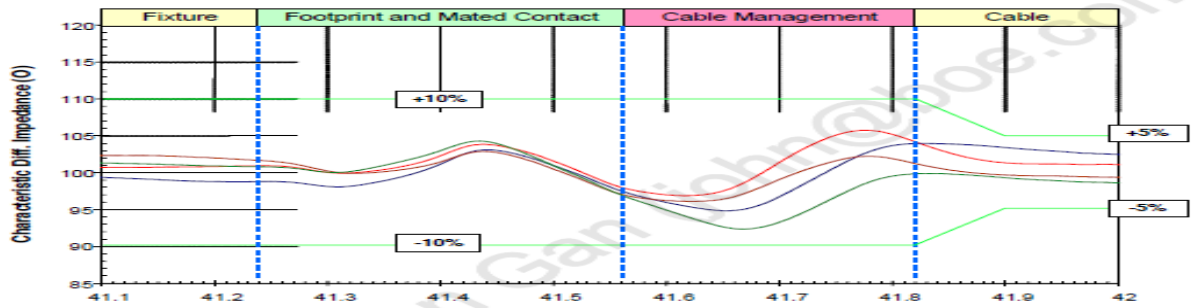
Eye for TP3 at RBR

Purpose

1. Main Link EYE Diagram should meet TP3 point of VESA.
2. The measure method is through access fixture.

Appendix C

## Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/85Ω VESA	±10%
Connector	100Ω/85Ω VESA	±10%
Wire management	100Ω/85Ω VESA	±10%
Cable	100Ω/85Ω VESA	±5%

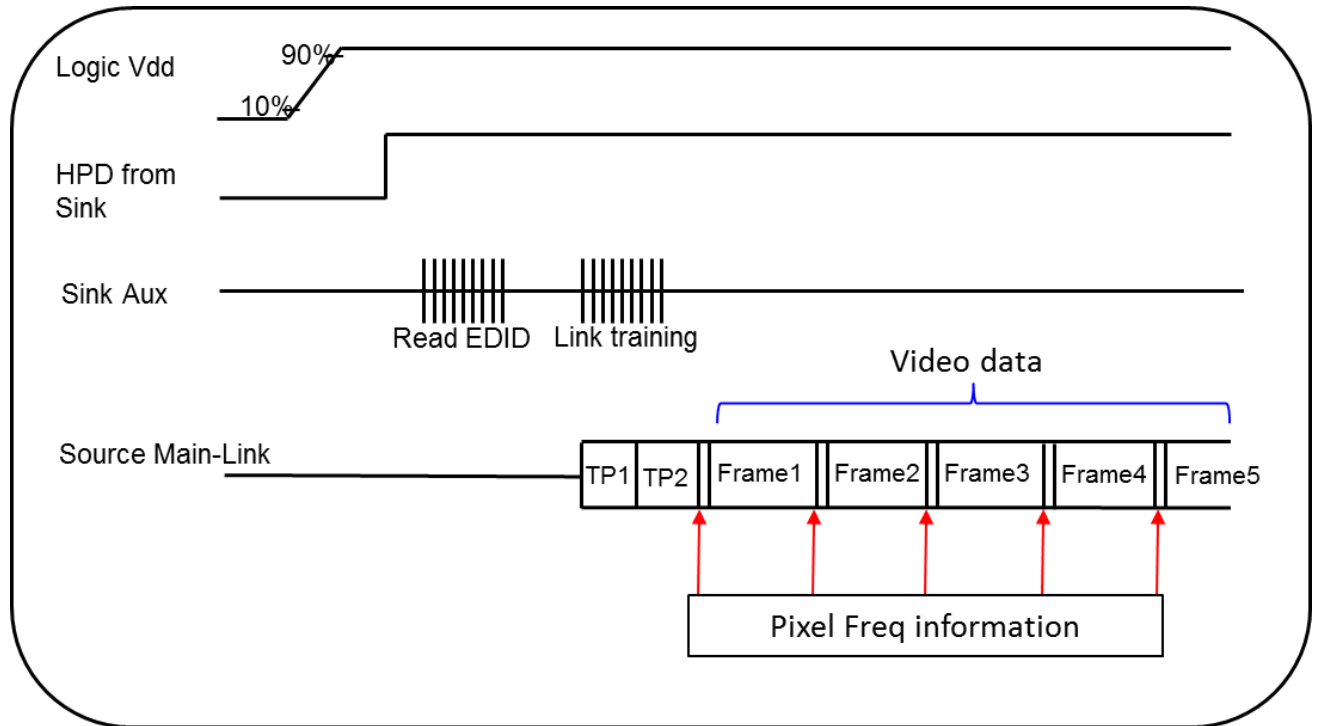
Impedance Profile Values for Cable Assembly

Purpose

Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

## Main Link Pixel Freq information value of MSA data

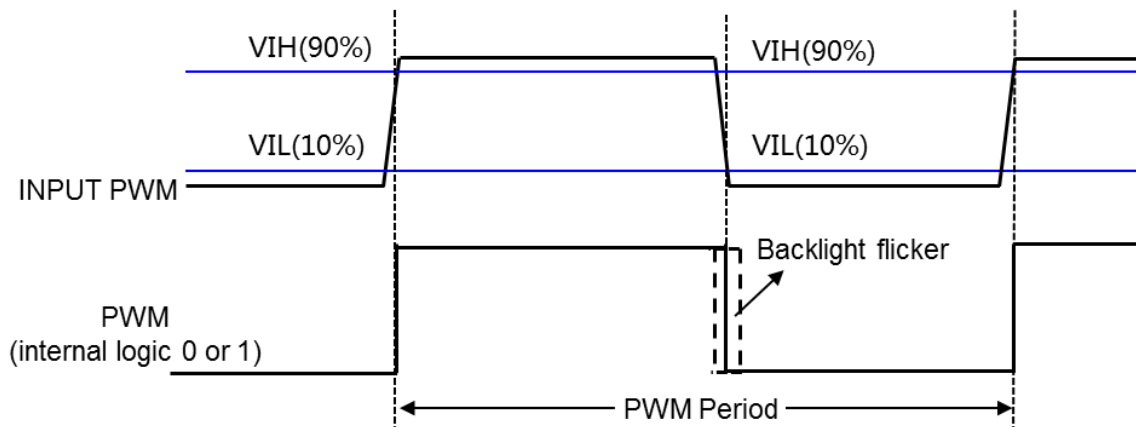


Purpose

1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on.
2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix C

**Main Link Pixel Freq information value of MSA data**



Example:

Freq	Cycle Time	PWM Rising Time	PWM Falling Time
200Hz	5ms	$\leq 1\mu s$	$\leq 1\mu s$
1KHz	1ms	$\leq 200ns$	$\leq 200ns$

Purpose

1. LED driver need to calculate the duty cycle of input PWM signal.
2. To avoid backlight flicker visible on LCD, system input PWM suggest :  
 $PWM \text{ rising} \leq 200ppm * \text{cycle time}$  ;  $PWM \text{ falling} \leq 200ppm * \text{cycle time}$ .